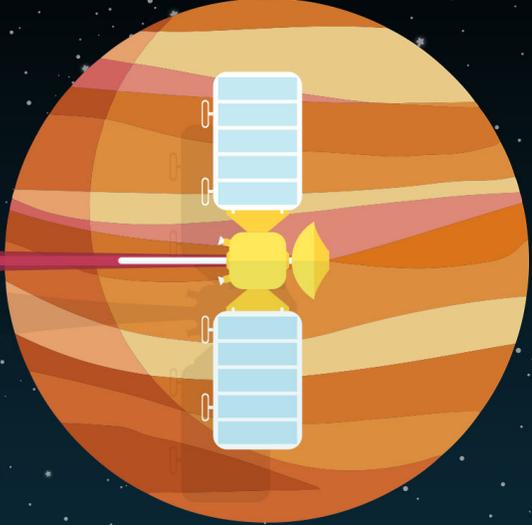


New Approaches to Assessing Reliability: COTS and More

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ANALYTICAL HEAVY LIFTING

# “Optimizing the Test - Analysis Ratio for Mission Success”



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Thursday, February 6, 2020

## *Optimizing Electronics Test/Analysis Ratio*

By **CHARLES HYMOWITZ**

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Electronics reliability can be assessed through test and analysis. Budget and time constrained programs often shun analysis as too expensive or challenging. In many cases, little to no analysis is performed. But is testing alone more cost effective in improving reliability?

Test tells us what is. Test has many potential pitfalls: bad data, bad equipment, bad interpretation. Test determines typical performance and requires parts to be produced prior to build. Test alone can miss specified requirements for beginning/end- of life, derived requirements, and is only valid for the measurement lot.

Analysis tells us what it could be. Analysis computes margins, risk, parameter sensitivity, and identifies fatal and rare events. Performance aspects are examined, quantified, and evaluated through a series of analyses (worst case circuit analysis, stress and derating, failure mode, effects and criticality analysis, and mean time between failures)

Targeted analysis should target tolerance ratios, heritage reference designs, and stress levels combined with failure modes analysis. Analysis problem discovery is in the derived requirements, minor design changes, signal integrity-power integrity, and at the interfaces/connectors.

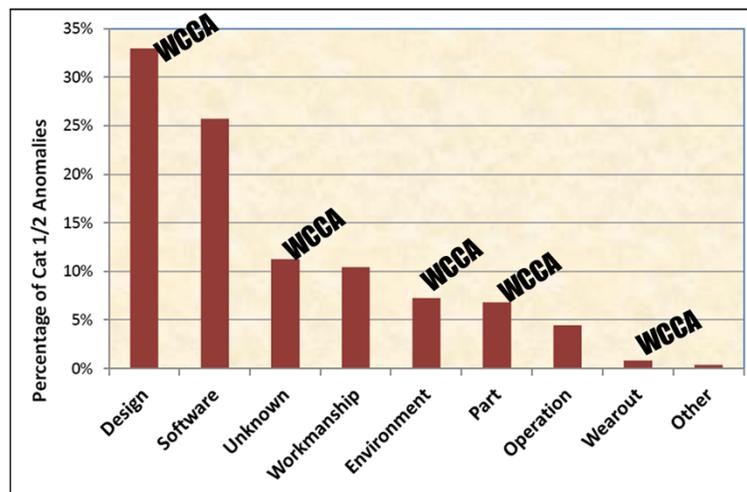
Check lists exist (TOR-2012(8960)-4\_Rev. A) with guidelines for selected application based on historical use and current needs. Analysis can gain confidence from nominal performance and limited statistical test data. Test and analysis make a powerful combination if applied complementary even when constrained.

– *Aerospace Getting It Right Newsletter*, <https://aerospace.org/getting-it-right>

# Overview

- **Many programs are test heavy. For some, no analysis is performed at all**
  - ❖ The reasons are varied, some valid most not; resources, cost, schedule, “we test”, the mission is short, etc.
- **Electronics reliability is a function of the amount of test AND analysis applied**
  - ❖ Presuming parts don’t fail and the design is manufactured well
- **What does test miss?**
  - ❖ Tolerance Stack-up (BOL, EOL), Mistakes (near misses), Design Centering, Derived requirements which are not usually tested, and Parameter sensitivities
- **So, how does analysis enhance testing and how much analysis do we need?**

As discussed in CubeSat Mission Status, 2000-present, 454 Spacecraft, CubeSat Database and “Gone too Soon? How successful are U.S. satellites at reaching their design life?” – Space Power Workshop 2014, Past data shows more analysis gives more reliability.



## Causes of high reliability electronics failures - first 3 years

“Proposed Common Data Views And General Trends From Anomaly Escape Assessment”, Aerospace Corp, 2009

WCCA addresses many areas critical to product quality including verification and validation. For Space applications, we are clearly not doing enough WCCA since 32% of early on-orbit failures are design related.

# Reliability Analyses

## WCCA

- Pin Down the Margins
- Assure Spec Compliance

- Functions...
- Stability
- Startup - Inrush
- Power Sequencing
- Signal Integrity
- Regulation

## Stress & Derating

- Improve Reliability
- Find Overstressed Parts

- Parts...
- Resistor Power Dissipation
- Diode Temperature
- FET Gate Voltage
- Inductor Current
- Transformer Saturation

## FMECA

- Determine the most critical failures
- Focus the WCCA Effort

- Short - Open
- Stuck
- Out-of-Tolerance
- Severity

## MTBF

- Rank Component Reliability and Failure Rates

- FIT Rate
- MTBF
- Parts Count/Stress Based

*“It is through this series of analyses that performance aspects of the system and design are examined, quantified, and evaluated.”*

There are four general electrical parts reliability analyses. The one focused on in this presentation is WCCA. WCCA is a functional analysis that includes both nominal and toleranced assessments.

Reliability analyses increase the likelihood that the design will meet the intended performance requirements throughout the product's lifetime and particularly at the End-of-Life (EOL). It is the objective of the WCCA to determine that the probability of circuit variations due to component parameter variations over life and environments are acceptably small. Stress and derating analysis is generally performed for both nominal and worst case operating conditions, in order to assure that all components are maintained within acceptable derating guidelines during all operating conditions. Most stress analysis, while labeled worst-case, is often not. Tolerances, power supply voltages, and circuit loading are not very often not fully EOL EVA.

### **The difference between these pseudo WC and fully WC can be an order of magnitude difference.**

Failure Modes and Effects Criticality Analysis (FMECA) shows what the system impacts would be for various failure modes in a system. The FMEA seeks to identify *Single-Point Failure Modes*. Ideally, an FMEA should be done down to the piece-part level of every circuit, but typically it only extends down to the functional block level. But without the Criticality portion of the assessment, the analysis isn't nearly as useful.

WCCA is substantively different from FMECA, but because the WCCA analysts become so familiar with the detailed operation of every circuit, it behooves them to be on the lookout for component failures that could cause a loss of redundancy (such as components in a cross-strapping circuit), and report any such findings to the FMECA analysts. Conversely, FMECA analysts should help the WCCA analysts determine which circuits are critical.

## Reasons to Perform Worst Case Analysis

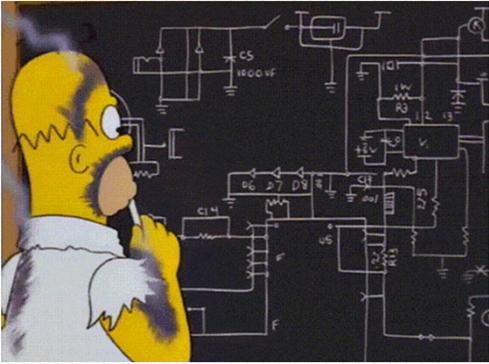
<b>Design Verification and Reliability</b>	To verify circuit operation and quantify the operating margins over part tolerances and operating conditions - Will the circuit perform its functions and meet specifications/To quantify the risk
	To improve performance - to determine the sensitivity of components to certain characteristics or tolerances in order to better optimize/understand a design and what drives performance
	To verify that a circuit interfaces with another design properly
	To determine the impact of part failures or out of tolerance modes
<b>Test Cost Reduction</b>	To evaluate performance aspects that are difficult, expensive or impossible to measure (e.g. determine the impact of input stimulus and output loading so as not to damage hardware)
	To set ATP limits
	To verify SATs/SITs and if they are needed/what their limits should be
<b>Parts Assessment</b>	To reduce the amount and scope of testing
	To determine if a part is suitable (too cheap, too expensive, right characteristics) or if a new technology can be used
	To support/set critical parameters and SCD requirements/screening definition
<b>Schedule, Cost, or Contractual Risk Reduction</b>	To perform Single Event Transient (SET) analyses
	To reduce board spins - determine the impact of late stage design or part changes
	To verify changes to heritage circuits
	To obtain better insurance rates or reduce contractual liabilities
	To avoid a catastrophic or costly incident

There are many reasons to do WCCA apart from reliability improvement.

The ROI is significant, especially if results can be reused and engineers learn from the process.

WCCA saves money and schedule by helping to reduce design iterations, board spins, returns/recalls, and other production and warranty processes that contribute to cost overruns.

# Why We Need Analysis



**“Reference” Designs and Design Recommendations Aren’t Vetted**



**Test & Vendor Data are often inconclusive**



**We’re Biased**

Reference design and design recommendations often lead us astray. They are meant to show off part features and/or provide generalized design guidance. They are almost NEVER vetted for worst case conditions, BOL or EOL tolerances, all PCB layouts, or all potential applications.

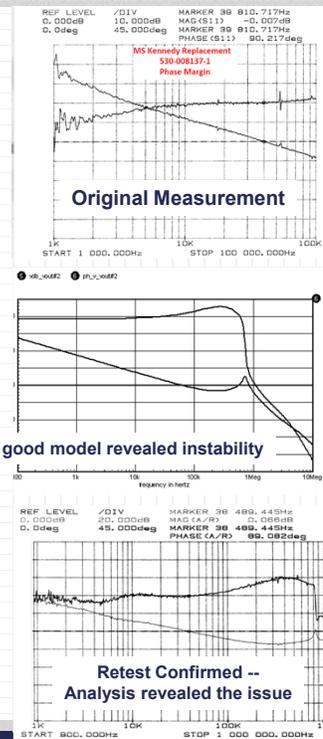
Module manufacturers are simply not doing the in-depth scrutiny and analysis we think they are. Or that they should be. Parts Vendors are killing us – every year data sheets have less data and often bad or outdated advice. Sample “canned” analyses are often performed to bogus, ill and undefined generic loading, invalidating most of the closed loop results. This leaves us wondering what the real worst case bounds are.

Test data often misses the mark for a variety of reasons as is discussed next.

Analysis performed in-house is usually not sufficiently rigorous. Companies, programs, and engineers suffer from a number of biases. This is why the Aerospace TOR and other guidelines recommend independence in the analysis process.

# Why Test Needs Analysis

- **First rule of test - Know what you expect to see**
  - ❖ How do you know the test data is good?
- **Where do the test limits come from?**
  - ❖ ATP limits come from analysis
- **We have become an industry of makers**
- **Test has many pitfalls**
  - ❖ Bad data, Bad equipment, Bad interpretation
  - ❖ Only determines typical/temp performance, not BOL
  - ❖ Requires parts to be procured prior to build
    - ✓ Only valid for the measurement lot
- **Testing isn't cheap, fast, or easy**



In many senses, we have become an industry of makers. Letting part vendors provide us with designs that are simply implemented without detailed verification and validation. The phrase, I just used the reference design is often the source of so many production problems. In many areas best practices don't work nominally let alone WC.

We don't test flight units to the same degree we test preliminary engineering hardware. Some limitations of the Testing-Only approach include:

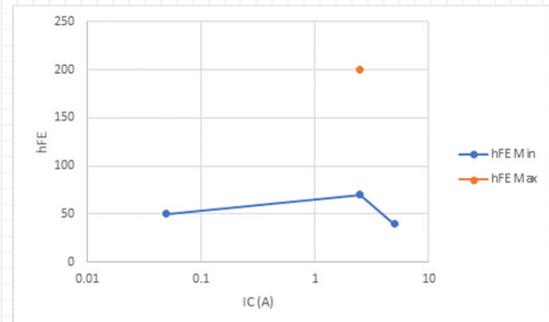
- Only determines initial 25C performance. Temperature testing may occur for some aspects but that still does not include all initial tolerances which is the LARGEST tolerance.
- Testing is only valid for the measured lot, many parameters vary significantly lot to lot and manufacturer to manufacturer
- Testing often requires the parts to be procured PRIOR to completion of WCCA, if any analysis is performed at all. THIS IS VERY RISKY!!
- Testing can be very costly if many measurements are required or the test is expensive to obtain.
- Engineering labs are often under-equipped, oscilloscopes often have insufficient bandwidth or memory
- Test setups are often inadequate, corrupted the measured data.
- Test data is often mis-interpreted



# There is no Nominal

- For many parts, no nominal data is provided or available
  - ❖ Mil-specs often only have min or max and, in many cases, only one side
- How do you test when there is no nominal?
- You don't know where your circuit sits – so how do you bound or evaluate performance?

BJT hFE Initial Mil-Spec Requirement



The device performance can be anywhere in between and/or outside these bounds

All you need to know about why nominal models aren't typical and why we need perform EOL EVA assessments

*“Remember you are dealing with a Fab that produces technology that was developed in the 80's and we don't have precise control over the lot-to-lot variability*

*When we target the device during fabrication, we need to put the gain curve inside the min/max parameters defined in the mil-prf-19500 slash sheet. So you could get devices that are almost anywhere within those limits.*

*Obviously, we try to stay away from the min's and max's because they will change after HTRB, Burn In, and Life tests, so we don't want to fail a lot because we were too close to the limits.*

*This is especially true for devices that we do not make that often and need to re-learn how to target the process every lot.”*

*-- Quote from Popular Rad-Hard Semiconductor Vendor*

# BOL vs EOL Tolerances

- Don't pare down to the bone unless you know where the bone is

Part Type	Parameter	Tolerances	Total EVA	Positive Ratio	BOL : EOL
Capacitors	C	Initial: -20% - +20%	-55.5% - 47%	Initial: 42.55%	3.7:1
		Temperature: -25.50% - +17.00%		Temperature: 36.17%	
Tantalum Capacitors	ESR	Aging: -10.00% - +10.00%	-99.82% - 3423.08%	Aging: 21.28%	100:0
		Radiation: 0%		Radiation: 0%	
Ceramic Capacitors	C	Initial: -10.00% - +10.00%	-91.00% - +46.00%	Initial: 21.74%	1.19:1
		Temperature: -60.00% - +15.00%		Temperature: 32.61%	
Diode	Vf	Aging: -21.00% - +21.00%	-100% - +314.45%	Aging: 45.65%	313.45:1
		Radiation: 0%		Radiation: 0%	
Op Amp	Vos	Initial: -44.12% - +86.21%	-6.50E-03 - +6.70E-03	Initial: 27.42%	2.94:1
		Temperature: -55.88% - +227.24%		Temperature: 72.27%	
Op Amp	Ibias	Aging: +1%	-9.705E-07 - +5.136E-07	Aging: 0.32%	2.733:1
		Radiation (10krad): -3.50E-04 - +5.00E-04		Radiation: 7.46%	
Resistors	Resistance	Initial: -4.05E-07 - +1.76E-07	+/-2.1% to +/-3.6%	Initial: 27.8%	0.8 : 1 to ~3.2 : 1
		Temperature: -4.05E-07 - +2.00E-07		Temperature: 38.94%	
55342K(100ppm) (1%)	Resistance	Aging: -4.05E-08 - +1.76E-08	+/-2.1% to +/-3.6%	Aging: 3.43%	0.8 : 1 to ~3.2 : 1
		Radiation (10krad): -1.20E-07 - +1.20E-07		Radiation: 23.37%	
55342K(100ppm) (1%)	Resistance	Initial: +/-1%	+/-2.1% to +/-3.6%	Initial: 27.8%	0.8 : 1 to ~3.2 : 1
		Temp: +/-0.6%		Temperature: 16.7%	
55342K(100ppm) (1%)	Resistance	Aging: +/-0.5% to +/-2%	+/-2.1% to +/-3.6%	Aging: ~20% - 55.6%	0.8 : 1 to ~3.2 : 1
		Radiation: +/-0%		Radiation: 0%	

Ratio of BOL to EOL
0.8 : 1 to ~3.2 : 1

This table shows the EVA tolerance stackup for various types of parts, as well as the BOL (initial/temp) to EOL (aging/radiation) ratio. In some cases, mil-spec manufacturing and other environmental tolerances are not included. Aging includes storage, test, integration, and flight time. It should be noted that parts age unbiased.

It is important to note the ratio. While most of the variance is BOL, many parts, such as resistors, can have equal or greater EOL drift. The resistance variations are due to different aging tolerances (from different guidelines).

The take-away is as noted in the slide. You should not pare down to the bone (tolerance-wise) because we don't know where bone is. When EOL tolerances can be substantial, test does not corral performance.

# BOL vs EOL Tolerances

- Test retires risk, but not all and not in all cases

Transistors	Parameter	Tolerances	Total EVA	% Positive Ratio	Ratio of BOL to EOL
2N7616UB	VGSth	Initial: 15% Temp: 25% Aging: 10% Radiation: 15%	65%	Initial: 23% Temp: 38% Aging: 15% Radiation: 23%	1.6 to 1
2N2222AUB	hFE at Ic=15	Initial: 75 Temp: +149.03, -34.87 Aging: 10 Radiation: -22.23	+234, -142.1	Initial: 32% to 53% Temp: 25% to 64% Aging: 4.3% to 7.0% Radiation: 0% to 16%	3.4:1 to 22.4:1
	Vcesat	Initial: 200% Temp: 24% Aging: 15% Radiation: 10%	+249%	Initial: 80.32% Temp: 9.64% Aging: 6.02% Radiation: 4.02%	8.96:1
	Vbesat	Initial: 30% Temp: 8.1% Aging: 15% Radiation: 10%	63.1%	Initial: 47.54% Temp: 12.837% Aging: 23.772% Radiation: 15.848%	1.524 to 1
Voltage References	Parameter	EOL EVA	Total EVA	% Positive Ratio	Ratio of BOL to EOL
REF02A	Vo	Initial: 0.3% Temp: 0.05% Aging: 0.06% Radiation: 0.20%	0.61%	Initial: 49.18% Temperature: 8.20% Aging: 9.84% Radiation: 32.79%	1.346 to 1
Voltage Regulators	Parameter	EOL EVA	Total EVA	% Positive Ratio	Ratio of BOL to EOL
ISL75051SEH	Vadj	Initial: 0.5% Temp: 0.5% Aging: 0.19% Radiation: 0%	1.19%	Initial: 42.017% Temperature: 42.017% Aging: 15.966% Radiation: 0%	5.263 to 1

# COTS Impact on WCCA

	COTS	Automotive	Mil-Spec
Simulation Models	Very limited, varies by popularity	Good and supported	Some, but very poor quality and no support
Part Data	Good	High Quality	Very Limited, Limits only Few graphs
Support	None	Non-existent for Space	Limited
Cost	Low	Low	Very High
Tolerances	Limited	Detailed	Limited data, screening available
Rad Performance	Unknown	Unknown	Defined for key parameters



- **WCCA doesn't care where the parts came from - COTS doesn't change the WCCA scope needed**
- **The less we know about the parts we use the more analysis we need**
- **MORE WCCA generally needed for COTS due to uncertainties**
- **Part Tolerances are the Key, Not the Part Pedigree**

We don't know a lot about the parts we use. We may think we do, but there is usually a surprise inside. And like the candy Cracker Jack's, you don't know the surprise until you open the part and look inside (at the detailed performance drivers).

Because of the wider and/or often more undefined tolerances in COTS parts, WCCA is even more essential. The uncertainty lends itself to more WCCA.

# The Current State of Power Integrity

**“Power is not my problem, its yours.”**

-- high speed designer

<https://www.youtube.com/watch?v=crLZTirpeXs>

**“What do you want, I gave you 5Vdc?!?!”**

-- power supply designer

**Dirty Secret: They're both wrong.  
Power is everyone's problem.**



<https://www.youtube.com/watch?v=crLZTirpeXs>



**Power Supply Designers & Manufacturers**

**PCB Designers**

**Digital Load Designers**

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Power integrity (PI) is simply the assurance that power applied to a circuit or device is appropriate for the desired performance of the circuit or device.

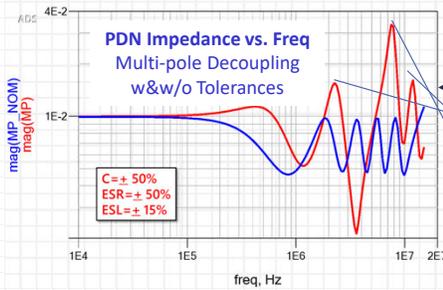
The current state of power integrity awareness is where signal integrity was 10-15 years ago. This is currently one of the biggest, if not the biggest design issue at the moment. Its ramifications are widespread and issues are very challenging.

There are many factors contributing to poor power integrity design practices. There is blame all around from part manufacturers, to power supply designers, to board layout, to the digital load designers.

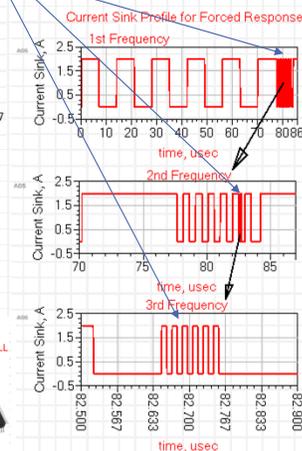
This is a big topic and there are many good papers, app notes, webinars, and videos. If you are interested in being part of the solution and learning about good PI design practices, please contact AEI Systems (Charles@aeng.com) directly for more information.

# The Basic Problem: How we get into trouble

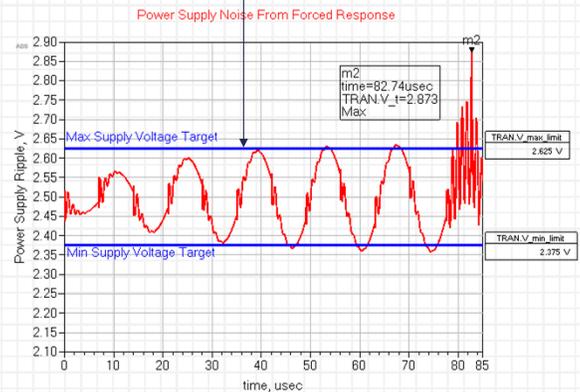
*Reference Designs - Ugh!  
Best Practices – Ha!*



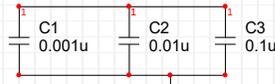
But this is what we build!



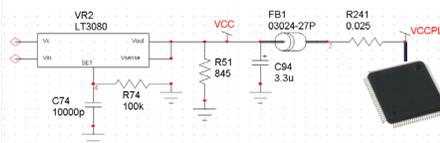
**This is the Goal**



Per decade decoupling



Beads



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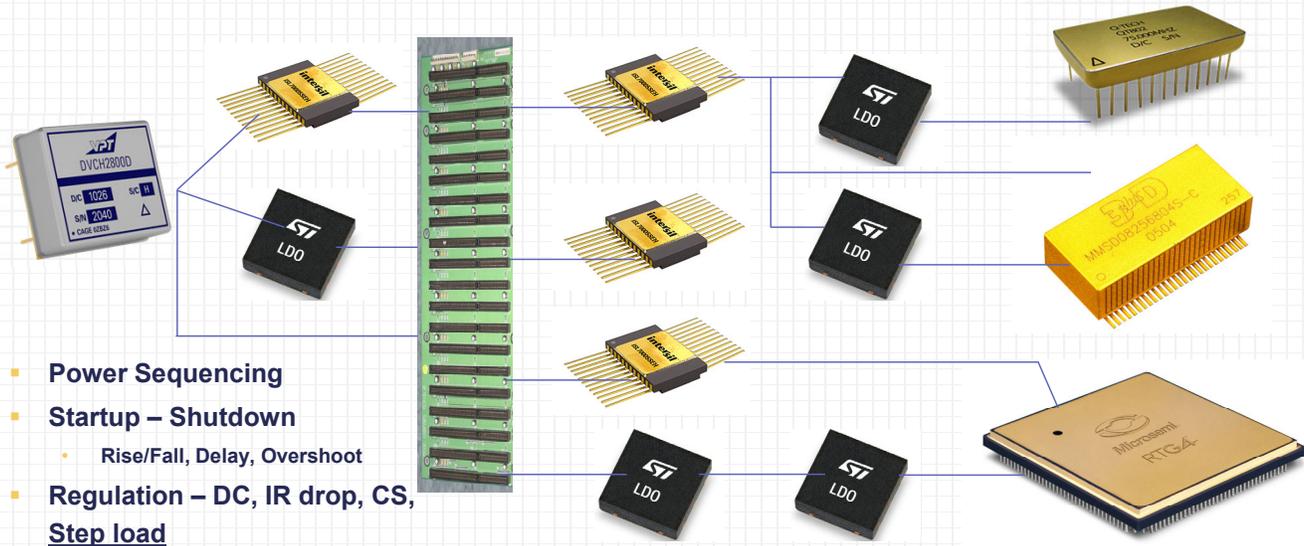
Voltage regulation windows are getting smaller. DC regulation, PSRR, ripple, IR drop, and voltage excursions must all fit in this ever-shrinking window.

Part vendor recommendations are often wrong and lead us into problems. There are many great articles on why beads and per decade decoupling should not be used. Tolerances exacerbate impedance variations.

The impedance peaks pose a problem. One impedance peak results in a voltage transient when subjected to a dynamic load current. When more than one peak is present it is possible to arrange the current transient in such a way as to stack the transients on top of each other. The resulting voltage transient is much bigger than the transient resulting from a single resonant peak. These excessive voltages can cause circuits to malfunction and, in some cases, can result in permanent damage due to the excessive voltage transients.

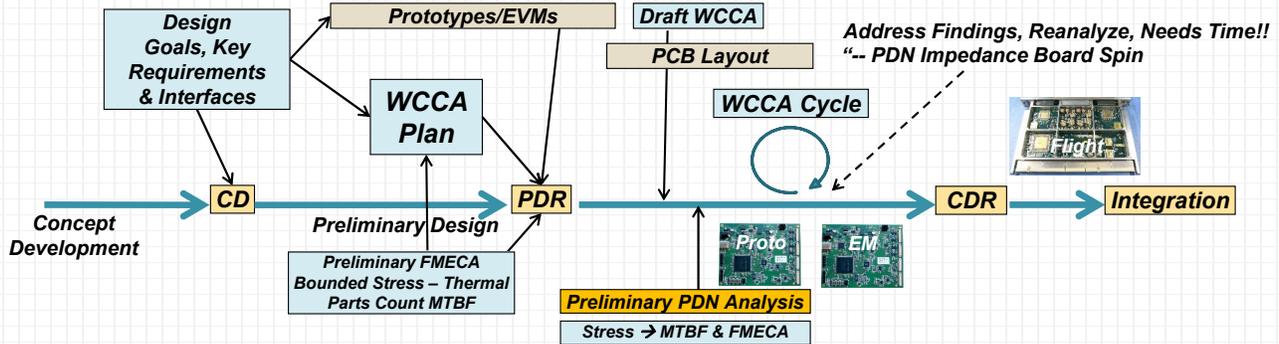
This is a great video series on the topic: <http://www.tinyurl.com/pi-videos>

# Power Distribution System



- Power Sequencing
- Startup – Shutdown
  - Rise/Fall, Delay, Overshoot
- Regulation – DC, IR drop, CS, Step load
- Stress, EMI, Thermal

# Integrating Test and Analysis



- **Keep Impedance Flat - Meet Target Impedance**
- The performance of FPGAs, CPUs, and other high-speed logic devices is directly dependent on the PDN
- No where is simulation more essential then in Power Integrity
  - ❖ Testing is very challenging
  - ❖ Dynamic currents are unknown and PCB spins aren't practical to fix issues
  - ❖ 3D FEA to include PCB effects is essential
- Even with analysis, a board spin is almost always desirable

WCCA is often shoe-horned between the end of the design process and the critical design review.

Prototype or EM hardware may be fabricated before the analysis is complete and its recommendations can be implemented. Power Integrity, in particular, needs to wait for analysis and a board spin is usually needed to get it right.

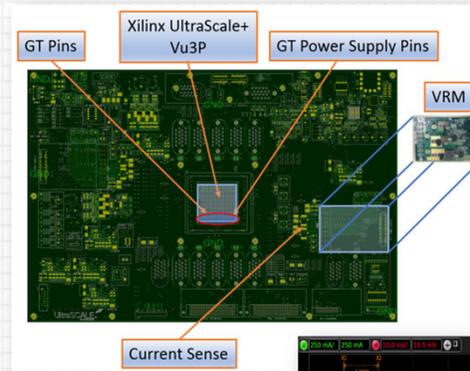
Without an analysis, there is virtually no chance that the power integrity will be adequate.

WCCA also often understaffed. Unfortunately, too many projects find themselves still designing right up until the design review and beyond and there is little or no time to properly perform the WCCA, let alone address the outages found.

This is potentially disastrous. The WCCA needs time to be completed properly and outages need to be resolved. Otherwise, most of the value of the analysis is wasted.

# Where Analysis Finds the Most Problems

- **Power Supplies**
  - Filter Stability, Q
  - Startup, Regulation
  - Stability
  - Sequencing
- **Derived Requirements**
- **Simple Circuits**
- **“Minor” Design Changes**
- **Reference Designs**
- **Signal Integrity – Power Integrity**
- **Interfaces - Connectors**
- **Part Overstress**



**20-40% of first pass WCCA is non-compliant**



On average, first pass analysis reveals that 20-40% of the requirements assessed do not pass and reveal findings. This is over AEi Systems history of 20+ years and hundreds of WCCAs.

**Derived Requirements** - circuits that do not have specifications but have to work for the functional block to work

- Stability
- Current Limit
- FET Gate Drive - BJT leakage and minimum hFE
- Opamps in unity gain configurations

## Simple Circuits

- High 'Q' Circuits, Filters, LC using ceramics, Beads
- Relays
- Opto-couplers
- Voltage and Zener References

## Signal & Power Integrity

- SSO Noise, PDN Resonances → Regulation
- Monotonicity
- WC Timing
- Logic Compatibility, improper terminations

# What is the right ratio?

- **Analysis can be targeted**
  - ❖ Depends on what is tested (EM vs Flight)?
  - ❖ What functions could drift?
    - **Derived quantities are often not tested**
      - Stability, gate drive, power sequencing
  - ❖ Is BOL – EOL drift significant? (Mission Life/Radiation)
  - ❖ How safe are Heritage - Reference Design – DS Recommendations
  - ❖ Did you assess worst case stress? Stress → most bang for reliability buck
  - ❖ Did you do the FMECA?
- **Check lists exist (TOR and other guidelines)**
- **The PROCESS of analysis gives us insight – It corrals biases**

# Conclusions

- **Test and Analysis Go Hand-in-Hand**
  - ❖ They Support Each Other
  - ❖ The 'right' ratio is not 100% Test – 0% Analysis
- **Need to target historical problem areas**
- **Mind the tolerance stackup – even for short missions**
- **Companies, Programs, and Designers are Biased**
  - ❖ They greatly overestimate the confidence gained from nominal performance and limited statistical test data

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